69. The method of claim 68, wherein ~~said storing~~ comprises storing texels in linear cache lines ~~of said texture~~ cache.--

REMARKS

By the foregoing Amendment, claims 1-41 have been canceled and new claims 42-69 have been added. These changes are believed not to introduce new matter, and their entry is respectfully requested.

Based on the above Amendment and the following Remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections, and that they be withdrawn.

Rejections under 35 U.S.C. §102

At paragraphs 2-11 of the Office Action (Paper No. 10), the Examiner rejected claims 1-19, 25, 28, 29, 31, 37, and 40 as being anticipated by U.S. Patent No. 5,790,130 to Gannett ("Gannett"). In accordance with the amendment above, Applicants have canceled claims 1-19, 25, 28, 29, 31, 37, and 40. The rejection of claims 1-19, 25, 28, 29, 31, 37, and 40 is therefore rendered moot. Applicants reserve the right to argue the merits of canceled claims 1-19, 25, 28, 29, 31, 37, and 40 in future prosecution.

Rejections under 35 U.S.C. §103

At paragraphs 14-19 of the Office Action (Paper No. 7), the Examiner rejected claims 26, 27, 30, 38, 39, and 41 as being unpatentable over Gannett, and at paragraphs

20-24, the Examiner rejected claims 20-24 and 32-36 as being unpatentable over Gannett in view of U.S. Patent No. 5,945,997 to Zhao et al. ("Zhao"). In accordance with the amendment above, Applicants have canceled claims 20-24, 26, 27, 30, 32-36, 38, 39, and 41. The rejection of claims 20-24, 26, 27, 30, 32-36, 38, 39, and 41 is therefore rendered moot. Applicants reserve the right to argue the merits of canceled claims 20-24, 26, 27, 30, 32-36, 38, 39, and 41 in future prosecution.

New Claims 42-69

New claims 42-69 recite elements of a texture storage system according to the present invention.

In the Office Action, the Examiner relies on Gannett for the teaching of a texture cache. Applicants note, however, that the cache system of Gannett is fundamentally different as compared to the texture cache of Applicants' invention. Gannett's texture cache includes cache lines that store 256x256 texels. *See*, col. 14, lines 10-11 of Gannett. Assuming two bytes per texel, the cache lines would hold 128KB of data. In Applicants' system, on the other, hand, an example cache line would store 64 texels. *See*, page 17, lines 9-13 of Applicants' specification. Assuming two bytes per texel, Applicants' cache lines would therefore store 128B of data.

As can be appreciated, the cache lines as contemplated by Gannett are much larger as compared to the cache lines of Applicants' invention. This difference is indicative of a fundamental distinction in the type of texture cache that is being implemented. More specifically, Gannett's texture cache is interrupt driven, wherein data transfers to the texture cache are controlled by the CPU. *See, e.g.*, col. 8, line 51 to col. 9,

line 29 of Gannett. Applicants' texture cache, on the other hand, is state-machine driven, wherein data transfers to the texture cache are controlled by the direct memory access engine. *See*, pages 9-10 and FIG. 2 of Applicants' specification. For at least these reasons, Applicants submit that claims 42-61 are patentable over Gannett.

In another aspect of the present invention (claims 62-69), a storage mechanism is provided that stores two-dimensional data in memory using an address that is formed by interleaving individual bits of values of a coordinate in a first dimension with individual bit values of a coordinate in a second dimension. *See,* pages 15-17 and FIGS. 5 and 6 of Applicants' specification. In the preferred embodiment, the texels are stored in linear cache lines that are accessible using an address formed by interleaving individual bits of values of texture coordinates in the 'u' and 'v' dimensions. In general, this storage process maintains the positional relationship of texels in the texture cache, thereby providing rapid access to texel values.

At paragraph 21 of the Office Action (Paper No. 10), the Examiner relied upon Zhao for the alleged teaching of storage of texels in cache lines. In particular, the Examiner relied upon the following excerpt that states:

> Texture cache 802 stores portions of texture map 101 on a square-by-square basis by providing a plurality of cache lines 604, each of which is capable of storing data describing one square 601. In the example shown, 16 bits 603 are shown in each cache line 604, corresponding to the 16 texels in a square 601.

See, col. 14, lines 5-13 of Zhao. As illustrated in FIG. 5 of Zhao, the 16 bits of square 601 are mapped into the cache line on a row-by-row basis. This row-by-row storage mechanism precludes the individual texels within square 601 from being accessed using an address formed by interleaving the values of the coordinates in two dimensions. For at

least this reason, Applicants submit that Zhao does not teach Applicants' cache line storage feature.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections, and that they be withdrawn. The Examiner is invited to telephone the undersigned representative if an interview might be useful for any reason.

Dated: 9/5/00

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